IN THE UNITED STATES
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PATENT APPLICATION

Ashok V. Krishnamoorthy

CASE   32

TITLE   Power Distribution Network For Optoelectronic Circuits

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

NEW APPLICATION UNDER 37 CFR § 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

>   Specification
>   4 Formal Sheets of drawing(s)
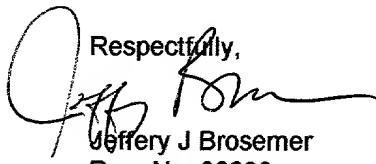>   1 Assignment(s) with Cover Sheet
>   Declaration and Power of Attorney

CLAIMS AS FILED				
	NO. FILED	**NO. EXTRA**	**RATE**	**CALCULATIONS**
Total Claims	11 - 20 =	0	x $18 =	$0
Independent Claims	3 - 3 =	0	x $78 =	$0
Multiple Dependent Claims, if applicable			+ $260 =	$0
Basic Fee				$760
			TOTAL FEE	**$760**

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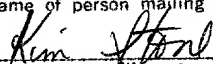
The Assistant Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR § 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

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Respectfully,

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Power Distribution Network for Optoelectronic Circuits

Field of the Invention

This invention relates generally to a power distribution network for
5   optoelectronic circuits and more particularly, to a power distribution tree
network for optoelectronic devices, such as vertical cavity surface emitting
lasers (VCSELs).

Background of the Invention

10   Vertical Cavity Surface Emitting Lasers have been widely used in a
variety of commercial products, including optical disc players and laser printers.
Furthermore, because VCSELs have lasing cavities that are perpendicular to
the optical surface of a laser chip, they can have a high packing density.
Therefore VCSELs have a promising future in high density laser arrays and
15   optical communication systems characterized by high data transmission rates
and/or high parallel processing speeds as well as a technology well-suited to
provide fast and high capacity data transmission between individual electronic
chips.

It is expected that the ability to directly integrate VCSELs onto CMOS
20   Optoelectronic-VLSI (OE-VLSI) chips can significantly reduce the cost of
deploying OE-VLSI technologies in high-performance systems.

OE-VLSI technology provides close integration of optical devices with
VLSI electronics. The goal is to supply multiple high-performance optical input
and output signals, with aggregate data-rates up to, and even exceeding, a
25   terabit-per-second to state-of-the-art VLSI circuits. Such technology allows a
significant increase in integration density over all-electrical systems because
the functionality present in many separate electronic chips can be condensed
into fewer chips (and in some cases a single chip) with large numbers of optical
inputs and/or outputs (I/Os).

30   Although VCSELs have recently been integrated into gigabit-per-
second CMOS OE-VLSI chips (see, for example, an article entitled "Vertical-

cavity surface emitting lasers flip-chip bonded to gigabit/s CMOS circuits," written by A. V. Krishnamoorthy et al., published in *IEEE Photonics Technology Letters*, Vol. 11, No. 1, January 1999.), many challenges remain before VCSEL-based OE-VLSI circuits can be reliably operated. In particular, the

5 problem of imprecise bias voltage across an OE-VLSI chip must be resolved, which results in VCSEL output power variations. Specifically, when a VCSEL is biased above a threshold, a small difference in bias voltage between two identical VCSELs in different locations of an array of VCSELs on an OE-VLSI chip can result in a large difference in light output power. Therefore, there is a

10 clear and present need for an effective means of maintaining a constant bias voltage across each VCSEL on an OE-VLSI chip.

Summary of the Invention

The problem of maintaining a constant bias voltage associated with

15 distributing a power signal to optoelectronic devices in an optoelectronic circuit is reduced or overcome by a power distribution network in accordance with the principles of the invention. The power distribution network includes electrically conductive pathways that form at least one level, where each level includes a plurality of equal-length conductive segments (hereinafter referred to as

20 "segments"), a means for coupling the power signal from a primary input to a point at the center of a first level, terminal nodes coupled at the extremities of a last level for supplying the power signal to devices that form at least a portion of the optoelectronic circuit, and wherein the number of segments connecting the primary input to each of said terminal nodes is equal. Since the length of

25 the conductive pathways from the primary input to each terminal node is equal, greater bias voltage uniformity is provided to the terminal nodes. A similar distribution network is used for the ground connection.

In one illustrative embodiment, the power distribution network for optoelectronic circuits includes electrical conductive pathways that form an H-

30 tree network that distributes a power signal to a plurality of terminal nodes (leaf nodes), for example, VCSELs on an optoelectronic chip. The H-tree network

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includes a primary input for receiving a power signal and conductive pathways that are arranged to form a plurality of levels, wherein portions of said conductive pathways are interconnected. Each level has a plurality of segments (branches) that forms at least one Arabic letter "H"-shaped pattern

5 (hereinafter known as "H pattern"). Each H pattern includes six equal length segments, with two segments in each of two parallel portions and two segments connected perpendicular at the midpoints of the parallel portions to form the H pattern). The pluralities of segments are laid out in a hierarchical succession of H patterns to form the various levels of the H-tree network. The first level is

10 coupled to the primary input, at the midpoint of the two perpendicular segments of the H pattern. A new level of the H-tree is formed by coupling the center of the two perpendicular segments of the new level H patterns to the end points of the preceding level H patterns of the H-tree. Terminal nodes are coupled to the end points of the last level of the H-tree. In this manner a conductive pathway

15 is formed from the primary input to each terminal node, with portions of each conductive pathway interconnected with one or more other conductive pathways. Since the length of each segment is equal for a respective level, the length of the conductive pathway from the primary input to each terminal node is the same.

20 In operation, the power distribution tree network utilizes the equal lengths of the conductive pathways of the H-tree network to provide greater bias voltage uniformity to the terminal nodes by eliminating small differences in bias voltage to terminal nodes in different locations of the optoelectronic circuit. The differences in bias voltage result from resistive voltage drops along a

25 conventional linear power supply line. Although, bias voltage uniformity at each terminal node is improved, the current consumption of other terminal nodes may affect the overall bias voltage stability (due to the shared conductive pathways).

In another illustrative embodiment, the power distribution network

30 includes an H-tree network, which is configured in an H-tree geometrical pattern that ensures that the absolute voltage at each terminal node is not

affected by the current consumption of other terminal nodes in the optoelectronic circuit. The H-tree geometrical pattern is similar to the embodiment described above except that each terminal node has a separate conductive pathway associated with it. Specifically, the conductive pathways

5   from the primary input to each terminal node are not shared for any portion of the pathway. Each conductive pathway is equal in total length but is joined to other conductive pathways only at a common point.

Brief Description of the Drawing

10   The invention will be more readily understood after reading the following detailed description taken in conjunction with the accompanying drawing, in which:

FIG. 1 is a graph of the output power of a VCSEL bonded to an OE-VLSI chip plotted as a function of input current;

15   FIG. 2 is a graph of the current-to-voltage relationship of the VCSEL of FIG. 1;

FIG. 3 is a schematic diagram of one illustrative embodiment of a power distribution network in accordance with the principles of the present invention;

20   FIG. 4 is a schematic diagram of another embodiment of the power distribution network in accordance with the principles of the present invention; and

FIGS. 5 and 6 are diagrams of other geometrical patterns for a tree network that can be used with a power distribution network in accordance with

25   the principles of the present invention.

Detailed Description

The present invention is an arrangement for distributing power to optoelectronic devices on an optoelectronic circuit, for example, an array of

30   VCSELs integrated into a VLSI chip, using a novel power distribution tree

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network. The tree network utilizes equal lengths of conductive pathways to each optoelectronic device to distribute power. The tree network eliminates small differences in bias voltage to the optoelectronic devices in different locations on the optoelectronic circuit resulting from resistive voltage drops

5   along a conventional linear power supply line.

In a typical VLSI chip, the power distribution network is a power-ground supply line or power bus, which is used to power many different circuit components by the same power bus. The power bus is generally two parallel power-ground conductive pathways (e.g., wires), fabricated from a conductive

10   material. The conductive material, typically metal, has an innate resistance. As will be understood by persons skilled in the art, the resistance of a wire is inversely proportional to its thickness and is typically characterized as ohms per square. This resistance results in a finite voltage drop along the wire when it is carrying current. For example, aluminum power supply lines have a

15   resistance on the order of 0.05 ohms per square. Thus, for example, if a circuit element consumes 10mA, then the voltage-drop on the aluminum power supply line with a resistance of 0.05 ohms per square and 50 squares in length is 25mV. If the same power supply line powers many such elements, the current, and hence the voltage drop proportionately increases.

20   Although voltage-drops are not typically an issue for digital circuits or for low-current analog circuits, they can have a dramatic effect on the output power of optoelectronic devices and, in particular, VCSELs. We note that maintaining precise bias voltage across a chip is typically not an issue with digital circuits because these circuits are designed to be resistant to fluctuations in the power

25   supply. However, as will be understood by persons skilled in the art, a VCSEL, for example, has a very sharp dependence on the voltage across the device due to the so-called sharp light (output power)-versus-current characteristic of such devices. In particular, the combination of large current requirements for VCSELs and finite resistance of the power supply lines can lead to small power

30   supply differences (e.g. bias voltages) to VCSELs in different parts of the array that result in the large differences in light output power.

The graph of FIG. 1 plots the output power (in milli-watts) of a VCSEL bonded to an OE-VLSI chip as a function of input current (in milli-amps). As shown in FIG. 1 a small change in input current leads to a large change in output power. The graph of FIG. 2 plots the current-to-voltage relationship of

5   the VCSEL of FIG.1. Accordingly, when a VCSEL is biased above threshold (in this case 0.9mA and 1.43V, represented by respective dots 10 and 20 in FIGS. 1 and 2), a large change in output power results from a small change in applied voltage or current.

Thus, to maintain a constant level of output power for each VCSEL in an

10   array of VCSELs on an OE-VLSI chip it is particularly important to ensure (1) that the threshold currents and voltages of each VCSEL are identical (an OE-VLSI chip fabrication issue) and (2) that each VCSEL in an array is biased identically (a circuit design issue). The latter, in turn, relies on maintaining a constant voltage and current bias across the VCSELs.

15   FIG. 3 is a schematic diagram of one embodiment of a power distribution network in accordance with the principals of the present invention. The power distribution network includes an H-tree network 12, represented by the inter-connected conductive pathways in the Arabic letter "H" patterns, for distributing a power signal received from a primary input 18, wherein the

20   conductive pathways are arranged to form a plurality of levels. For example, a four-level H-tree is shown in FIG. 3, with level one represented by the one large "H", level two represented by the next largest four "H's" and so on. The first level is coupled to the primary input, at the center of the two horizontal segments of the H pattern. The conductive pathways distribute a power signal

25   to terminal nodes 16 (represented by circles and as further indicated in the upper right hand quadrant for a portion of the terminal nodes of FIG. 3) on VLSI chip 20, wherein the distance from the primary input to each terminal node 16 is equal. In this illustrative example, each terminal node 16 represents a VCSEL and its associated driver.

30   Each level of H-tree network 12 includes pluralities of conductive segments (branches) 22.. Each segment 22 is represented by the individual

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portions of each "H" pattern and as further indicated in the lower right hand quadrant for a portion of one plurality of segments of one level of the H-tree network of FIG. 3. Each "H" pattern includes six equal length segments, with two segments in each of two parallel portions and two segments connected

5 perpendicular at the midpoints of the parallel portions to form the H pattern. The pluralities of segments 22 are laid out in a hierarchical succession of H patterns to form the various levels of the H-tree network 12. Each level includes at least one H pattern.

A first level is coupled to the primary input, at the midpoint of the two

10 perpendicular segments of the H pattern. A new level of the H-tree is formed by coupling the midpoint of the two perpendicular segments of the new level H patterns to the end points of the preceding level H patterns of the H-tree. Terminal nodes are coupled to the end points of the last level of the H-tree. In this manner a conductive pathway is formed from the primary input to each

15 terminal node, with portions of each conductive pathway being shared between two or more terminal nodes. Since the length of each segment is equal for a respective level and the total number of segments to each terminal node is also equal, the length of the conductive pathway from the primary input to each terminal node is the same. A similar distribution network is used for the ground

20 connection (not shown).

Although the classical H-tree interconnected conductive pathway configuration is commonly used for equidistant electrical clock distribution in multiple CPU designs on single a VLSI chip, it has not been exploited as a power distribution method. Such prior art H-tree configurations used the equal

25 conductive pathway lengths of the H-tree branches to minimize timing skew in the arrival of clock pulses to various elements of the H-trees in high-speed clock distribution circuits. For example, see an article entitled Fisher and Kung, "Synchronizing Large VLSI Processor Arrays," published in *IEEE Trans. Comp.*, Vol. C-34, No. 8, pp. 734-740 (August 1985), by A.L. Fisher et. al.,

30 which investigated clock skew in large two-dimensional arrays clocked by an "H-tree" network. In contrast to the prior art, an H-tree interconnected

conductive pathway configuration is used for powering optoelectronic devices, such as VCSELs, on an OE-VLSI chip.

In operation of the present invention, the effect of voltage drops due to power supply line resistance are reduced when DC power is distributed to the

5   terminal nodes of on optoelectronic circuit, namely the VCSELs in an array of VCSELs of an OE-VLSI chip, with the H-tree power distribution network. Since the lengths of the conductive pathways to each terminal node are equal, there is greater uniformity of the voltage and current provided to each terminal node.

Advantageously, when the current draw of the array of VCSELs on an

10 OE-VLSI chip is so-called "balanced" (by balanced we mean that there is geometrical symmetry with respect to the VCSELs that are "on" or drawing current), the VCSELs in an array are biased identically. Specifically, the precise bias voltage seen by a specific VCSEL (terminal node) is dependent on the total current flowing into the specific segments (due to potential voltage

15 drops along the various segments). This current, in turn, depends on the current consumption of the immediate neighbors of the specific VCSEL. For example, when a greater number of VCSELs are "on" in one location of the array (for example, the VCSELs in the upper left hand quadrant of FIG. 3), more current is drawn in those segments of H-tree network 12. In turn, those

20 segments have a higher voltage (due to Ohms law), and thus the associated VCSELs have a higher bias voltage than those in the other quadrants of FIG. 3.

Therefore, when there is a geometrical symmetry with respect to the VCSELs that are "on" and those that are "off" on an OE-VLSI chip, the current draw is the same and any voltage drop in the power lines is common to all of

25 the VCSELs. Accordingly, the bias voltage to all of the "on" VCSELs is the same and the OE-VLSI chip is balanced. One example of a balanced OE-VLSI chip is when all of the VCSELs are "on". However, typically VCSEL operation on an OE-VLSI chip is not balanced, therefore, it is not guaranteed that all of the VCSELs will receive the same bias voltage.

30 FIG. 4 depicts another illustrative embodiment in which the power distribution network is configured in an H-tree geometrical pattern ensuring that

the absolute voltage at each terminal node is not affected by the current consumption of other terminal nodes on the H-tree network. FIG. 4 shows a two level H-tree power distribution network 30 that distributes power to a 4X4 array of terminal nodes 32 on VLSI chip 34, of course, other level and array

5   configurations are possible. Each terminal node 32 has a separate plurality of conductive segments 36 that forms a separate conductive pathway associated with a particular terminal node, and each conductive pathway conforms to a classical H-tree geometrical pattern, as described above. Although the conductive pathways are all equal in total length (e.g., the sum of all segments

10   to a particular terminal node), the conductive pathways for each terminal node are not completely inter-connected. In contrast with a classical H-tree configuration, the power supply lines are joined only at a common point 38 (root). The common point 38 is coupled to primary power supply input 40, for example, a power supply pad on the perimeter of the VLSI chip. The ground

15   distribution network is in a similar configuration (not shown).

Since the current draw will occur at the common point and all of the conductive pathways are equal in length, any voltage drop will be the same for all the terminal nodes. Thus, all of the terminal nodes on the optoelectronic chip will have the same bias voltage. In this manner, the current load or draw

20   for one terminal node does not affect the bias voltage of other terminal nodes. As a result, this H-tree power distribution network ensures that any voltage drop on the power-distribution conductive pathways is the same for all the terminal nodes, and each terminal node on the H-tree experiences the same bias voltage independent of the total current flowing on the conductive

25   pathways.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognized that there could be variations to the embodiments shown and those variations would be within the spirit and scope of the present invention. For example,

30   Figs. 5 and 6 show two other tree patterns for a power distribution network in accordance with the principals of the present invention. FIG. 5 shows an X-

shaped tree pattern and FIG. 6 shows a skewed H-tree pattern (of course, portions of the conductive pathways of a tree network utilizing these patterns may or may not be shared analogous to the embodiments of FIGs. 3 and 4). Moreover, a hybrid combination of any of the patterns shown in FIGs. 3 through

5   6 may be used as a tree network to deliver power to optoelectronic circuits. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.
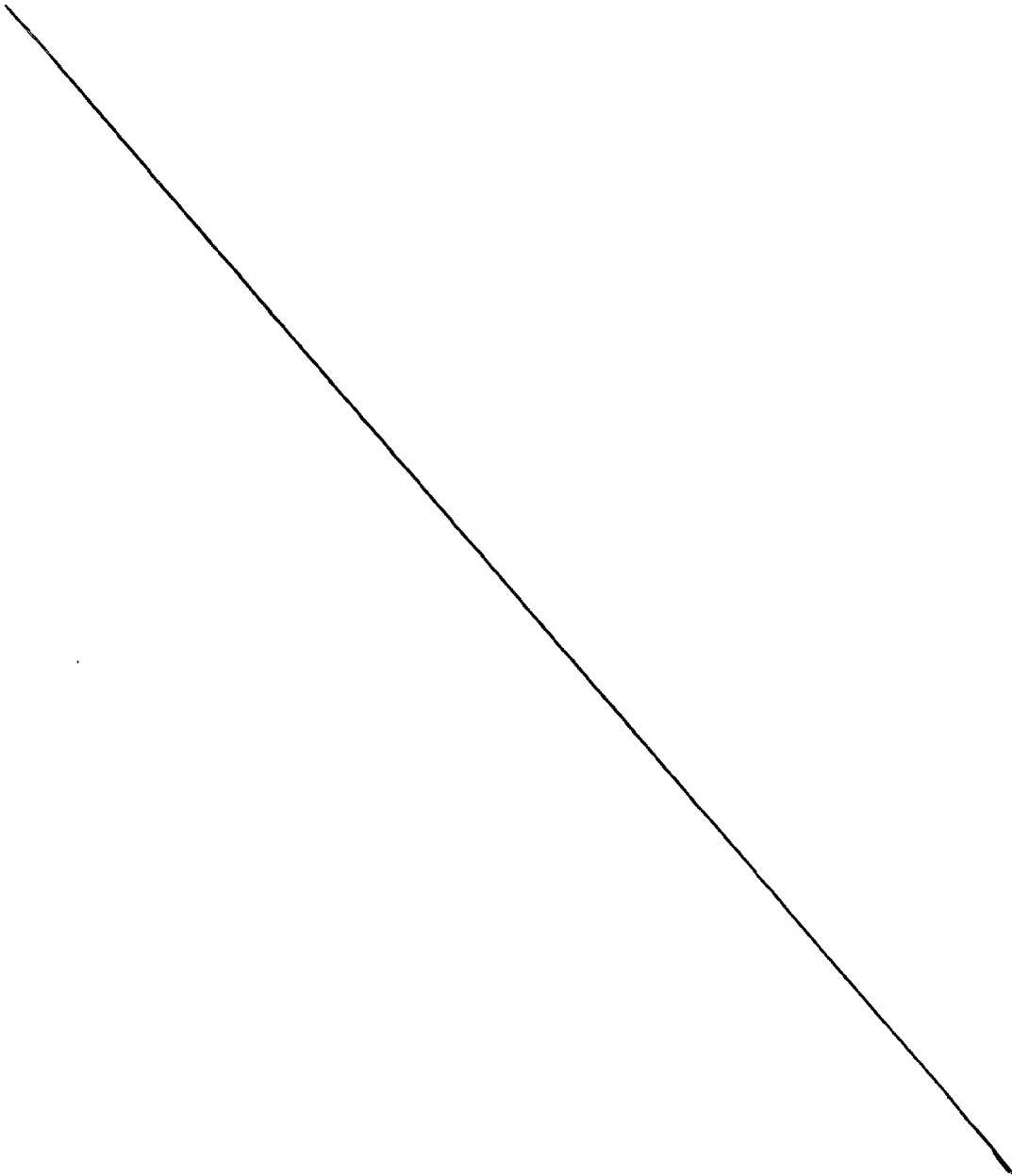
Claims:

1   **1.** A network for distributing a power signal in an optoelectronic
2   circuit, said network comprising:
3   a plurality of electrically conductive pathways forming at least one
4   level, wherein portions of said conductive pathways are interconnected;
5   a plurality of segments forming each level, wherein each segment of
6   a level is equal in length;
7   means for coupling said power signal from a primary input to a point
8   at the center of a first level;
9   terminal nodes coupled at the extremites of a last level for supplying
10   said power signal to devices that form at least a portion of said optoelectronic
11   circuit; and
12   wherein the number of segments connecting said primary input to
13   each of said terminal nodes is equal.

1   **2.** The invention defined in claim 1 wherein each level is at least one
2   H-shaped pattern comprising first and second parallel branches each having
3   a respective first and second midpoint, and a third branch interconnecting
4   said first and second midpoints, and wherein said center of said H-shaped
5   pattern is the midpoint of said third branch.

1   **3.** The invention defined in claim 1 wherein each level is at least one
2   X-shaped pattern comprising first and second branches each having a
3   respective first and second midpoint and interconnecting said first and
4   second branches at said midpoints, and wherein said center of said X-
5   shaped pattern is the intersection of said first and second branches.

1   **4.** The invention defined in claim 1 wherein said network is located on
2   an optoelectronic chip.

1   **5.** The invention defined in claim 1 wherein said terminal nodes are
2   optoelectronic devices.

1   **6.** The invention defined in claim 1 wherein said terminal nodes are
2   VCSELs.

1   **7.** A network for distributing a power signal in an optoelectronic circuit,

2   said network comprising:

3   a plurality of separate electrically conductive pathways forming at

4   least one level, wherein said pathways are joined only at a common point;

5   a plurality of segments forming each level, wherein each segment of

6   a level is equal in length;

7   means for coupling said power signal from a primary input to a point

8   at the center of a first level;

9   terminal nodes coupled at the extremites of a last level for supplying

10   said power signal to devices that form at least a portion of said optoelectronic

11   circuit; and

12   wherein the number of segments connecting said primary input to

13   each of said terminal nodes is equal.

1   **8.** The invention defined in claim 8 wherein each level is at least one

2   H-shaped pattern comprising first and second parallel branches each having a

3   respective first and second midpoint, and a third branch interconnecting said

4   first and second midpoints, and wherein said center of said H-shaped pattern is

5   the midpoint of said third branch.

1   **9.** The invention defined in claim 7 wherein each level is at least one

2   X-shaped pattern comprising first and second branches each having a

3   respective first and second midpoint and interconnecting said first and

4   second branches at said midpoints, and wherein said center of said X-

5   shaped pattern is the intersection of said first and second branches.

1   **10.** A method of distributing a power signal to a plurality of terminal

2   nodes on an optoelectronic circuit, the method comprising the steps of:

3   receiving the power signal from a primary input; and

4   directing said power signal to said plurality of terminal nodes using an

5   H-tree network, said H-tree network including at least one level, wherein a first

6   level is coupled to said primary input and a last level includes said plurality of

7   terminal nodes, each of said at least one level having a plurality of segments,

8   each segment of a respective plurality is equal in length; and

9   wherein a number of segments from said primary input to each of said

10   terminal nodes is equal.

1   **11.** The method of claim 10, wherein the directing step further includes

2   directing said power signal to said plurality of terminal nodes using an H-tree

3   network,

4   wherein said plurality of segments are configured into at least one H

5   pattern to form said at least one level; and

6   wherein said at least one level is configured into a hierarchical

7   succession of H patterns.

Abstract of the Disclosure

Method and arrangement are disclosed for a power distribution network for distributing power to VCSELS on an optoelectronic chip that maintains a constant bias voltage to the VCSELs. More particularly, the power distribution

5   network includes an H-tree network for directing a power signal. The H-tree network includes a primary input for receiving the power signal and at least one level, with terminal nodes coupled to the last level, and each level includes a plurality of segments. Each segment of a respective level is equal in length and the total number of segments from the primary input to each terminal node

10   is the same. Since the distance from the primary input to each terminal node is equal, greater bias voltage uniformity is provided to the terminal nodes. A similar distribution network is used for the ground connection.
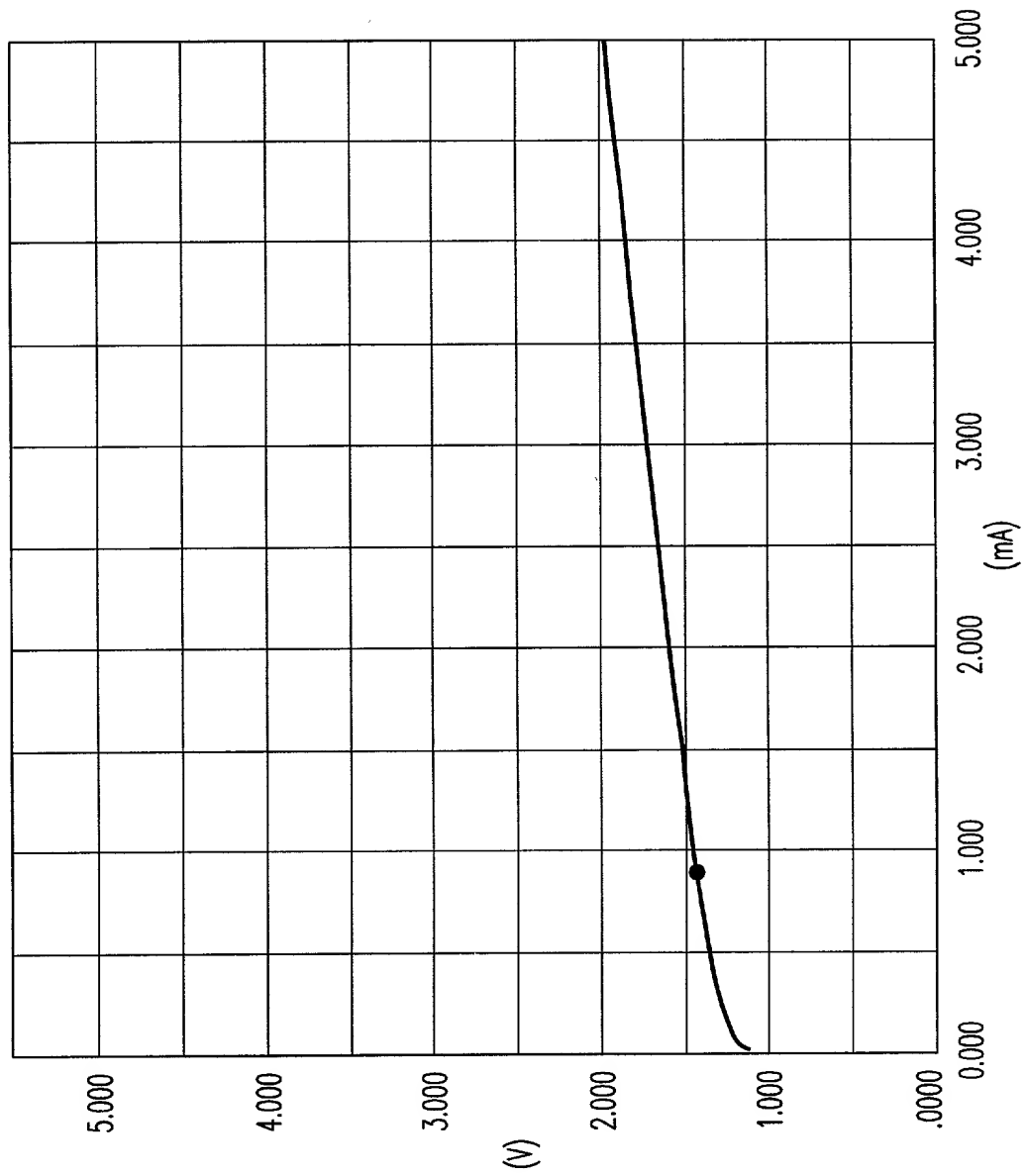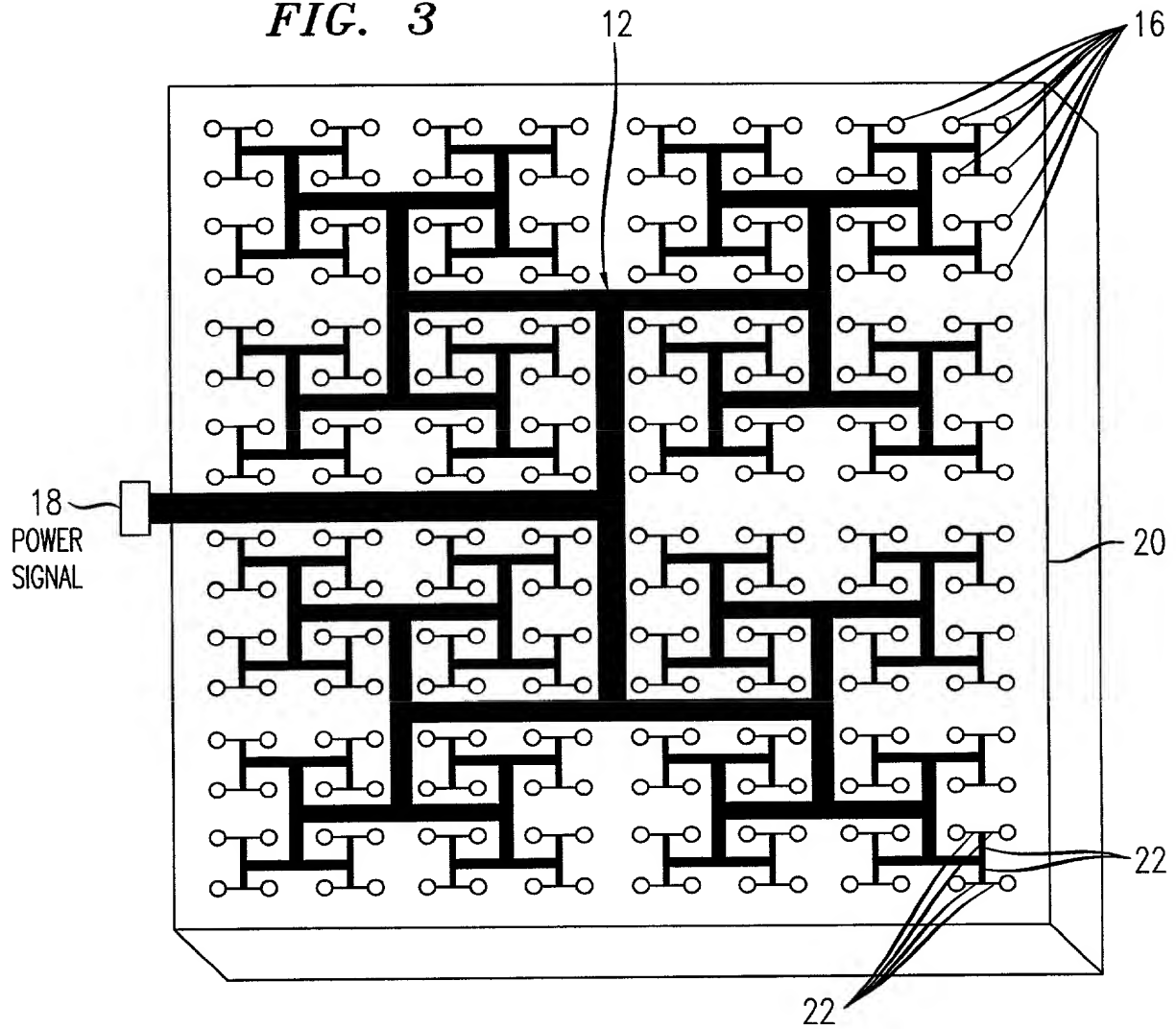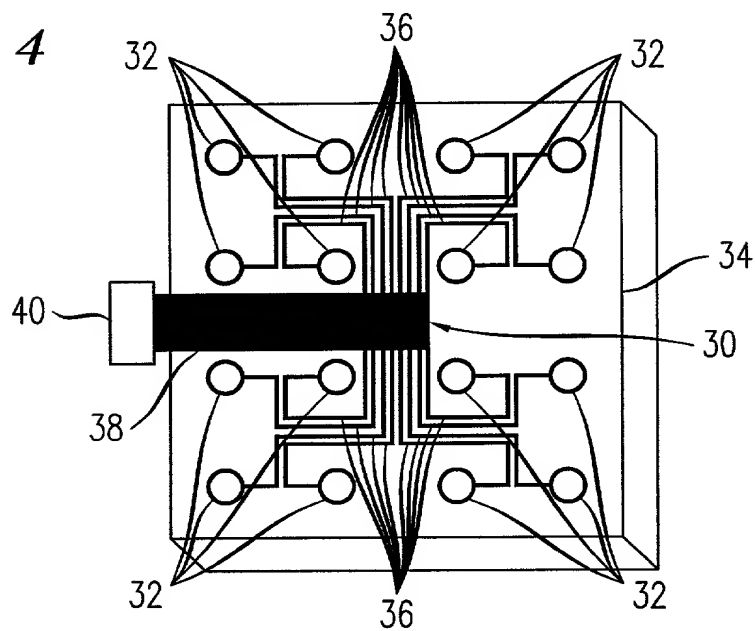
FIG. 1
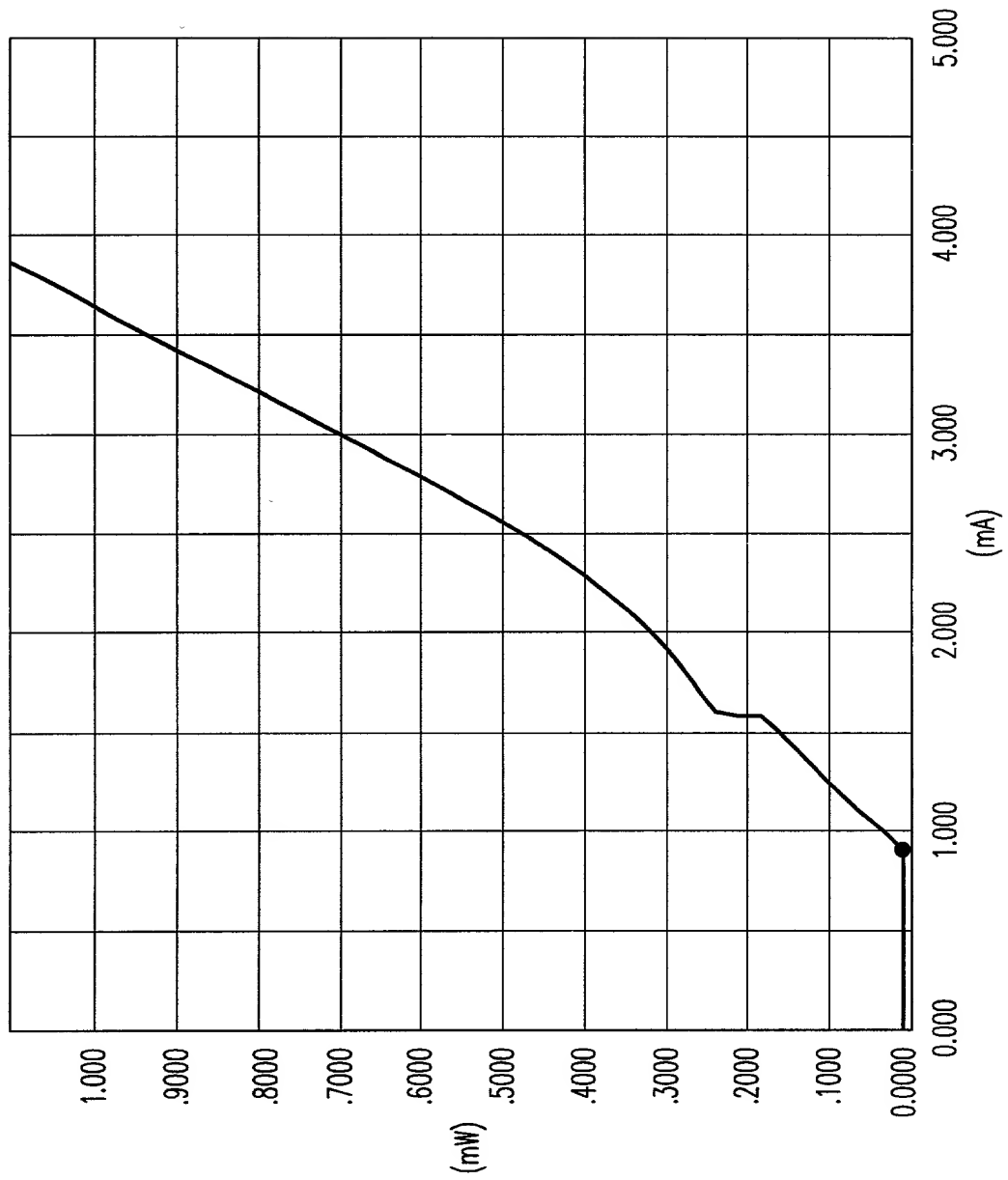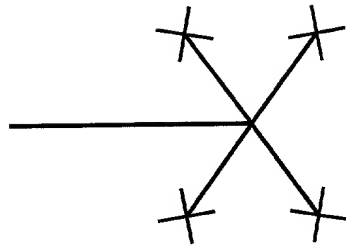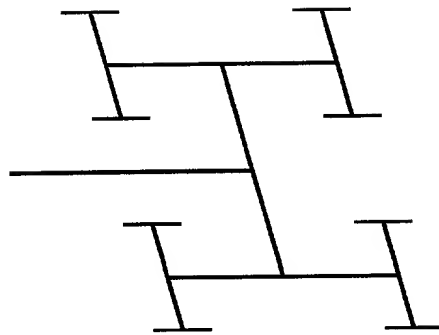
FIG. 2

FIG. 3

FIG. 4

FIG. 5

FIG. 6

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Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **Power Distribution Network For Optoelectronic Circuits** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

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